Item 12N FY96
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PURCHASE DESCRIPTION

ANALYZER, LOGIC

AN4NM-E

1.0 GENERAL This procurement requires a multichannel timing and state analyzer that can record and display logic signals and data from digital circuitry. The analyzer shall have specific probing and recording capabilities for an IEEE 488.1 logic interface.

2.0 CLASSIFICATION Type II, Class 5, Style E, and Color R in accordance with MIL-T-28800 for shipboard applications.

3.0 OPERATIONAL REQUIREMENTS The equipment shall be capable of both synchronous and asynchronous data domain and time domain recording of parallel digital signals as specified below. All specifications contained below shall be measured at the probe or lead tip used for connection to the unit under test.

3.1 Time Domain A timing format of at least 16 channels shall be recorded and displayed. Horizontal expansion capabilities shall be provided to display a portion of the total memory for more detailed examination. A positionable cursor that identifies recorded data words and time positions shall be provided. The triggering event shall be marked or annotated on the timing display. Operator assignment of the displayed channel order shall be provided.

3.2 Data Domain Displays of recorded data in binary, octal, and hexadecimal bases shall be provided.

3.3 Display Cathode ray tube. Minimum usable viewing area: 100 mm (4 in) high by 120 mm (5 in) wide.

3.4 Signal Inputs The analyzer shall be provided with a minimum of 20 separate signal input channels including probes, pods, cables, and other required accessories.

3.4.1 Data Channels. The analyzer shall have a minimum capability of receiving, recording, and displaying parallel data words of at least 16 bits in the timing and data domains, and shall be expandable to at least 32 bits.

3.4.2 Trigger Channels. The analyzer shall have at least two trigger qualifier input channels.

3.4.3 Clock Channels. The analyzer shall have an external clock input and a clock qualifier input channel.

3.4.4 Input RC: 100 kilohms minimum shunted by 8 pF or less

3.4.5 Threshold: The logic analyzer shall perform as specified when used to analyze TTL circuitry. The TTL threshold shall be 1.5 ±0.1V. The equipment shall be provided with a variable threshold, adjustable to within ±0.15V from -6.0V or less to at least +6.0V. High and low true logic polarity shall be selectable for each channel.

3.4.6 Maximum Input: ±30 Vdc referenced to ground

3.4.7 Input Modes

3.4.7.1 Sample Mode. The detected logic level present on each probe and at each clock transition shall be stored in the sample mode.

3.4.7.2 Latch Mode. Whenever multiple transitions occur between two successive clock intervals, the state opposite that stored during the previous clock interval shall be stored on the next clock. A glitch memory with corresponding glitch markers on the display may satisfy this requirement.

3.4.7.3 Minimum Pulse. In the timing and state modes, when the logic analyzer threshold is set for TTL in the latch or glitch modes, the equipment shall detect a 5 ns pulse with a level that changes from less than +0.25V to any amplitude from +2V to +5V and then returning to less than +0.25V. Detection shall also be provided for a 5 ns pulse with a level that changes from +2V to +0.83V or less and returning to +2V.

3.5 Internal Clock An internal clock with selectable periods from 10 ns or less to at least 50 ms shall be provided.

3.6 External Clock DC to at least 50 MHz with selectable positive and negative edge active modes.Minimum clock pulse width:10 ns or less.

3.6.1 Setup and hold time.12 ns or less

3.7 Memory At least 250 data word samples. A second memory of equal depth shall be provided for comparing word samples and searching for specific word occurrences within the recording memory.

3.8 Self-check A self-check function that verifies operation of all basic functions shall be provided.

3.9 Interface Probing The equipment shall be provided with a probing accessory and all required cables that allow the analyzer to record bidirectional data flow and the associated management signals required for IEEE 488.1 digital interface operation.

4.0 GENERAL REQUIREMENTS

4.1 Power source MIL-T-28800 nominal power source requirements are invoked. Maximum power consumption: 400 W.

4.2 Lithium batteries Per MIL-T-28800E, lithium batteries are prohibited without prior authorization. Requests for approving the use of lithium batteries, including those encapsulated in integrated circuits, shall be submitted to the procuring activity at the time of submission of proposals. Approval shall apply only to the specific model proposed.

4.3 Weight 20 kg (44 lb) maximum

4.4 Digital interface A digital interface shall be provided in accordance with MIL-T-28800. The equipment shall be capable of acting as an IEEE-488.1 controller and provide hard copy of data to an IEEE-488 compatible printer. In addition, a digital interface shall be provided in accordance with EIA-RS-232C and provide all the capabilities of the IEEE-488.1.